Subthreshold CMOS Implementation of the Izhikevich Neuron Model

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***Abstract*—Neuromorphic computing seeks to build hardware systems that are similar to the brain in form and function. Such systems are composed of artificial neurons and synapses, both of which will have to possess extreme energy efficiency to allow spiking neural networks to scale to the size of the brain. In this work, we present such a low-power subthreshold implementation of the Izhikevich neuron model, inspired by the circuit introduced by Wijekoon and Dudek. The circuit, designed in the UMC 65nm process, consumes 11.74fJ/spike at a 0.18V supply voltage, while operating on a biological timescale and allowing analog tunability of control voltages so as to exhibit different spiking behaviors. The circuit comprises an integrated digital spike transceiver that communicates with AER arbitration circuitry and generates reset pulses.**

***Index Terms*—Neuromorphic, SNNs, Izhikevich model, Subthreshold, CMOS, Low power**

I. Introduction

Spiking neural networks (SNNs) have recently become a popular candidate for the next generation of neural networks. This is mainly due to their biological plausibility, which could potentially provide insight into the actual functioning of the brain. Though modest SNNs can be simulated on digital computers, even the largest supercomputers of today are insufficient to simulate the entire human cortex in real-time. Exploitation of graphical processing units (GPUs) [4] and field-programmable gate arrays (FPGAs) [7] has led to some improvements but each of these systems are limited by the von Neumann memory bottleneck and it is unclear if they will ever reach an energy efficiency comparable to that of the neurons and synapses in the biological nervous system [5]. To address this problem, study into the field of neuromorphic engineering was started [1]. The principal focus was to build hardware that directly emulates the behavior of biological neurons and synapses by exploiting the similarity in behavior with transistors (particularly in subthreshold).

Various models of differing levels of complexity exist, from the simplistic leaky integrate-and-fire (LIF) model that is easy to implement in hardware, to the biophysically accurate Hodgkin-Huxley (HH) model [6]. The Izhikevich model [2] provides a good middle ground between these two because it can reproduce various neural activities while retaining computational simplicity.

Among the many CMOS circuits inspired by this model, the circuit proposed by Wijekoon and Dudek [3] has the simplest topology. However, their circuit operates in accelerated-time with a large supply voltage, which negatively impacts the energy efficiency. Although earlier works [18] have attempted to create equivalent circuits on biological timescales, they do not address the crucial issue of subsumption of the neuron circuit into a neuromorphic processor and how the arbiter signals and their corresponding delays would affect the function of the circuit.

In this work, we propose a subthreshold CMOS implementation of the Izhikevich model, based on the circuit proposed in [3], that operates on a biological time-scale, has an integrated digital subcircuit to communicate spikes to an AER arbitration system and provides an order-of-magnitude improvement in energy dissipation compared to the previously proposed circuits that operate on biological timescales [8]. Similar to the earlier implementation, the behavior of the circuit can be varied using two control voltages. The proposed digital spiking subcircuit also causes the circuit to be robust to arbiter signal delays and pulse widths, thereby enabling its use with digital circuitry that has variable routing delays.

In the next section, we describe the Izhikevich mathematical model. Section III provides a description of the functioning of the analog and digital subcircuits. Section IV lays out the simulation results and a comparison with earlier circuits. Section V concludes the paper.

II. Izhikevich Model

There is a large spectrum of mathematical models that attempt to describe the behavior of neurons. At one end of this spectrum is the HH model, which models ion channel conductances in a biophysically realistic way but requires highly complex circuitry to implement accurately. On the other end is the LIF model which is the simplest but cannot account for many observed behaviors, most notably frequency adaptation. The Izhikevich neuron provides a balance between the complexity of the HH model and the simplicity of the LIF model, serving as an ideal model for use with neuromorphic

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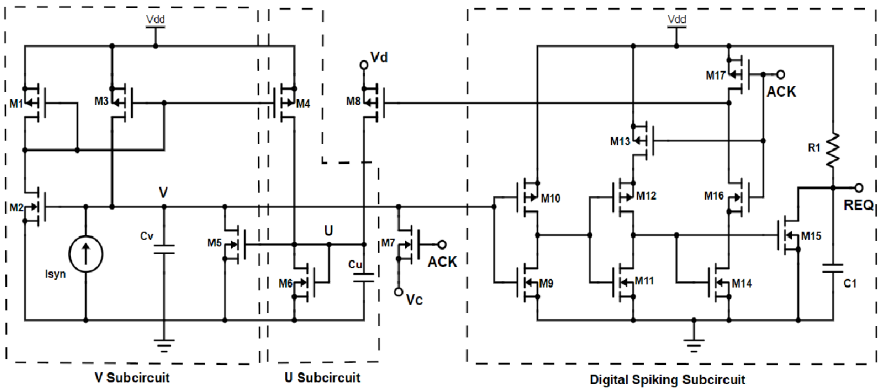

M1	300n/125n	**M12**	100n/100n
M2	300n/125n	**M13**	200n/100n
M3	300n/125n	**M14**	100n/100n
M4	650n/90n	**M15**	100n/250n
M5	400n/600n	**M16**	100n/100n
M6	700n/150n	**M17**	100n/100n
M7	175n/350n	**Cv**	20f
M8	1.3u/125n	**Cu**	300f
M9	100n/100n	**C1**	25f
M10	1u/100n	**R1**	200Meg
M11	1u/100n	**I_{syn}**	2p

Fig. 1. Circuit Schematic and Component Sizes

hardware. The mathematical description provided by Izhikevich is as follows:

$$\dot{v} = 0.04v^2 + 5v + 140 - u + I_{syn} \tag{1}$$
$$\dot{u} = a(bv - u)$$
$$v > 30mV : v \leftarrow c, u \leftarrow u + d$$

Where v is the potential difference between and interior and exterior of the soma of the neuron, commonly known as the membrane potential, and u is known as the 'slow membrane recovery variable' that accounts for the ion channel activations. The adjustable parameters a and b define the timescale for the recovery of u and the sensitivity of u to changes in v respectively. The parameters c and d are the reset voltage for v and the incremental reset for u respectively. I_{syn} is the sum of all input currents flowing into the soma of the neuron. Adjusting the values of a, b, c, and d allows the Izhikevich model to demonstrate different behaviors observed in biological neurons such as regular spiking, fast spiking, chattering, low-threshold spiking, intrinsic bursting etc [9].

III. Subthreshold Circuit Design

The proposed circuit is shown in Fig. 1. The circuit is split into 3 components as marked in the figure: the membrane voltage circuit, the recovery variable circuit, and the digital AER interface circuit that also generates the reset signals.

A. Analog Dynamics Circuit

The circuit operates in voltage-mode, with the state variables v and u being represented by the voltage across C_v and C_u respectively. The terms on the RHS of the differential equations in (1) are implemented using MOSFET drain currents as shown:

$$C_v \frac{dV}{dt} = I_{M3} - I_{M5} + I_{syn} \tag{2}$$
$$C_u \frac{dU}{dt} = I_{M4} - I_{M6}$$

Where I_{syn} is the input current to the circuit and I_{Mn} is the drain current of the n-th transistor. The circuit here uses a supply voltage of 180mV, which is well below the voltage required to cause strong inversion in the transistors. This ensures that all the transistors always operate in the subthreshold region.

Since the subthreshold currents follow an exponential relationship with the gate-source voltage, constraining their ranges appropriately allows us to realize linear and quadratic functions that are necessary for the Izhikevich model. A crucial factor to note is that the coefficient of the second-degree term in the v equation (0.04) is much smaller than the coefficient of the linear term (5). This is advantageous as the Taylor series coefficients also follow a similar trend, with successive coefficients becoming smaller. This constraint process can be thought of as an extension to linearization around the operating point of a MOSFET.

B. Digital Spiking and AER Circuit

The spike generation and communication functions are performed by the digital circuitry shown on the right in Fig. 1. When the membrane potential reaches the threshold of the inverter (M9, M10), the output of that inverter goes low. The ACK signal is normally low and hence the second inverter (M11, M12) remains activated, and its output goes high. This then turns on M14, and M15, which sends out an active-low request (REQ) signal to indicate that a spike has been generated to the following digital arbitration circuitry. The resistor R1 and capacitor C1 are used to emulate the load that M15 will have to drive. When the arbitration circuit sends back an acknowledge (ACK) signal that the spike has been processed, the membrane voltage is set to its reset voltage, V_c, via M7. Furthermore, M8 is turned on by ACK going high, which increases the voltage at U. The ACK signal also temporarily disables the second inverter through M13, to prevent any extraneous spikes from being sent out before the previous spike has been processed completely. M16 prevents the shorting of the supply during the waiting period between the time when REQ is sent out and the time when ACK is received. When the ACK pulse ends, the circuit has been reset to its original state and the temporal evolutions of state variables resume.

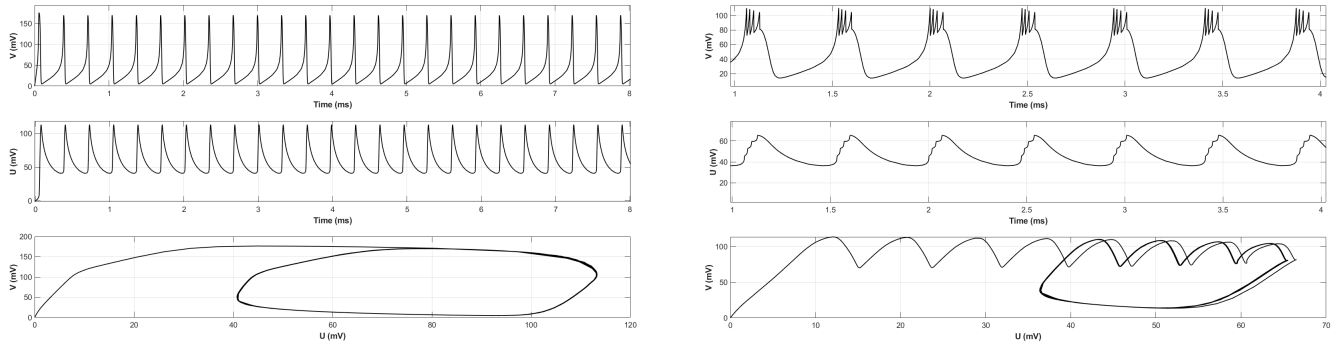

Fig. 2. Regular Spiking and Chattering Behaviors

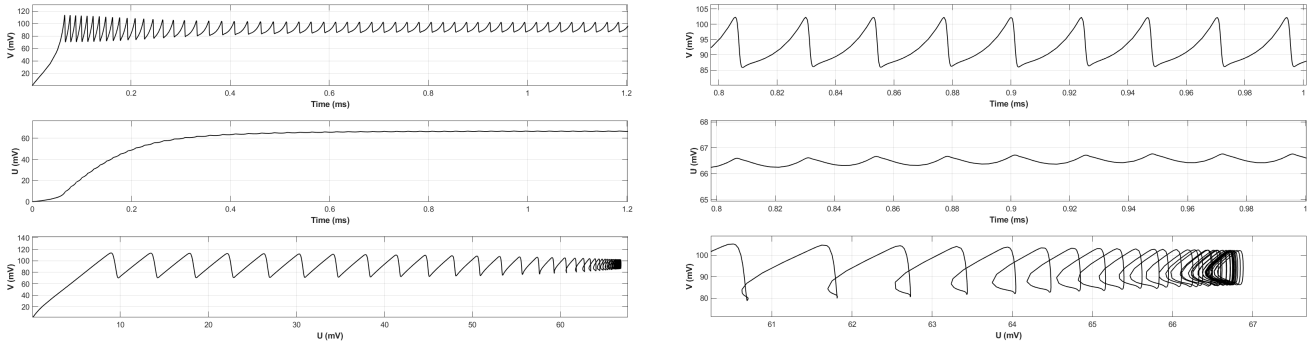

Fig. 3. Low Threshold Spiking, with the final periodic behavior zoomed in

IV. Results

The proposed Izhikevich neuron circuit was simulated in Cadence using the UMC 65nm technology node. Simulation results are shown in Figs. 2 and 3. Regular spiking (RS) was obtained by setting Vc to 140mV and Vd to 140mV. Chattering (CH) was obtained by setting Vc to 20mV and Vd to 150mV. Low threshold spiking (LTS) was obtained by setting Vc to 20mV and Vd to 20mV. An input current of 2pA was used for all three cases. For all these simulations, a 1μs delay was used between the time the REQ signal is sent out and the ACK signal is received to emulate the delay in the digital circuitry.

The regions of operation of the circuit are shown in Fig. 4, with X representing the regions where there is no spiking activity. The parameters Vc and Vd were varied in steps of 10mV each to generate data points.

Fig. 5 shows the variation in spiking frequency under two different control voltage settings, both in the RS mode, with the width of the ACK pulse that is used to reset the state variables in the circuit. The spiking frequency is practically constant over a range from $1ns$ to $10\mu s$, beyond which it drops gradually as the width becomes a significant proportion of the spiking time period itself.

Table I shows the comparison of this work with previously published circuits. Compared to the original circuit, which operates in accelerated time (microsecond scale), the circuit

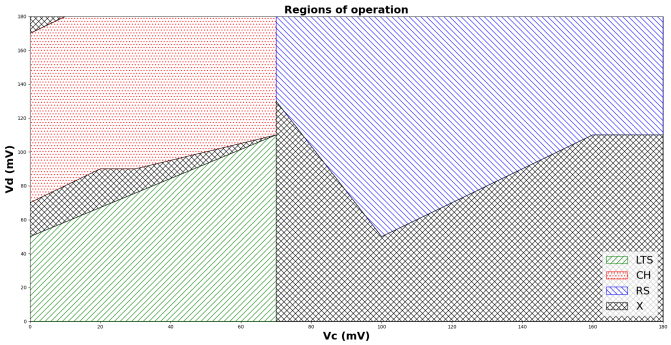

Fig. 4. Regions of Operation of the circuit. V_c and V_d are varied in steps of 10mV.

presented here shows activity on the millisecond scale, which is similar to biological neurons. Furthermore, it is possible to slow the firing rates even more by changing some transistor sizes. The circuit also achieves an energy consumption of 11.74fJ/spike in the regular spiking mode, which is the lowest reported for an Izhikevich model so far. Energy consumption for the different modes are shown in Table II.

Fig. 6 shows the variation in spiking frequency of the circuit in different modes, with varying input current. The frequencies are averages over a 5ms window to ensure a meaningful value for the circuit in CH mode, where the instantaneous frequency

TABLE I
PERFORMANCE COMPARISON

Parameters	This work	Dudek '08 [3]	Ronchini '20 [18]	Tamura '19 [12]	Rangan '10 [13]	Zhang '17 [14]	Braindrop '18 [15]	Loihi '18 [16]	TrueNorth '14 [17]
Model	Izhikevich	Izhikevich	Izhikevich	Izhikevich	Izhikevich	Izhikevich	Quad. IF	LIF	Aug. LIF
Implementation	Mixed	Analog	Analog	Analog	Analog	Mixed	Mixed	Digital	Digital
Technology	65nm	350nm	180nm	65nm	90nm	65nm	28nm	14nm	28nm
Timescale	Biological	Biological	Biological	Accelerated	Biological	Accelerated	Biological	NA	Biological
Energy (J/spike)	11.74f	8.5p	58.5f	2p*	1p	40f*	380f	24p	26p

∗Calculated from reported Regular Spiking frequency and power consumption values.

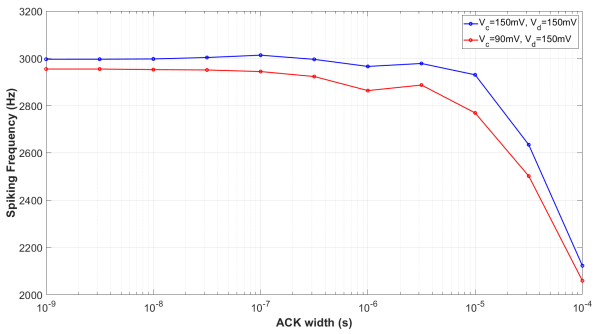

Fig. 5. Variation in Spiking Frequency with ACK signal width. Input current was fixed at 2pA.

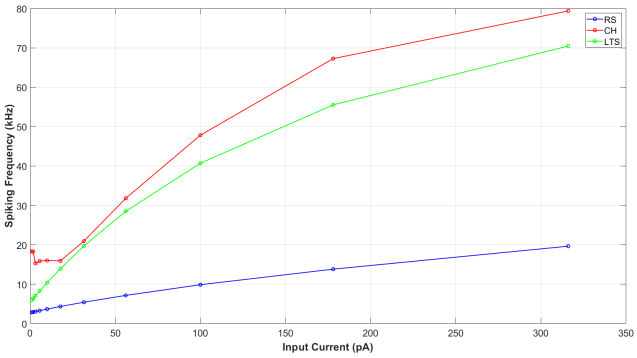

Fig. 6. Variation in Spiking Frequency with input current

is not constant across time.

Mismatch simulations were performed for the entire circuit, with a maximum of 10% variation in all lengths and widths, with all operation region boundaries shifting by less than 10mV in either direction. Capacitors were not varied in this simulation. Noise simulations, with contributions from all FETs resulted in a <0.1% timing jitter.

TABLE II
ENERGY CONSUMPTION

Operation Mode	Energy/spike
RS	11.74 fJ
CH	15.12 fJ
LTS	3.10 fJ

V. CONCLUSION

A subthreshold CMOS implementation of the Izhikevich neuron model was presented. The circuit, designed in the UMC 65nm process displays many of the spiking modes described by the model and achieves an energy consumption of 11.74fJ/spike, which is a significant improvement over the previous state of the art. The novel spike-generation block allows the circuit to operate reliably over 4 orders of magnitude of communication latencies. In contrast to previous implementations [18], the circuit operates reliably over a large area in the parameter space, allowing continuous tuning of parameters, resulting in a wider range of achievable spiking frequencies. The circuit, in its current form, does not exhibit the intrinsically bursting (IB) and thalamo-cortical (TC1) modes, but these spike signatures are very similar to low-threshold spiking and regular spiking respectively and hence will have nearly the same impact on a network. It is also pertinent to mention that none of the analog implementations demonstrate all the Izhikevich modes. Due to the extremely low energy consumption and supply voltage requirements, the circuit is suitable for use in large-scale spiking neural networks, neuromorphic processors and in embedded applications, like neuromorphic implants and ECG anomaly detectors, where power is a serious constraint.

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